Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently amended) An electronic interconnection system comprising:

a printed wiring board (PWB) comprising a first surface having at least a first contact pad and a second contact pad;

a chip package comprising a chip and a package substrate for the chip, wherein the chip is mounted onto the package substrate and the package substrate has a first surface having at least a first contact pad and a second surface having at least a second contact pad;

an electrical connection between the package substrate and the PWB, the electrical connection for coupling the first contact pad of the PWB with the first contact pad of the package substrate; and

a bridge lead for coupling the second contact pad of the PWB with the second contact pad of the package substrate.

2. (Original) The system as defined in claim 1, wherein the chip is mounted to the second surface of the package substrate.

3. (Canceled)

4. (Original) The system as defined in claim 1, wherein the bridge lead comprises at least one flying lead style of bridge lead.

5. (Original) The system as defined in claim 1, wherein the bridge lead comprises at least one edge wiping style of bridge lead.

6. (Original) The system as defined in claim 1, wherein the bridge lead comprises at least one top wiping style of bridge lead.

7. (Original) The system as defined in claim 1, wherein the bridge lead comprises at least one double wiping style of bridge lead.

8. (Original) The system as defined in claim 7, wherein the bridge lead further comprises a heat sink and thermal interface material for extracting heat from the chip.

9. (Original) The system as defined in claim 7, wherein the bridge lead further comprises at least a portion of an integrated Electro-Magnetic Interference shield for the chip.

10. (Currently amended) The system as defined in claim 1, wherein:

the first surface of the PWB is substantially parallel to the first surface of the package substrate;

the first surface of the package substrate is substantially parallel to the second surface of the package substrate; and

the chip is mounted on the second surface of the package substrate~~; and~~

~~the electrical connection comprises a solder ball~~.

11. (Original) The system as defined in claim 10, wherein the bridge lead comprises at least one top wiping style of bridge lead.

12. (Original) The system as defined in claim 10, wherein the bridge lead comprises at least one double wiping style of bridge lead.

13. (Original) The system as defined in claim 12, wherein the bridge lead further comprises a heat sink and thermal interface material for extracting heat from the chip.

14. (Original) The system as defined in claim 12, wherein the bridge lead further comprises at least a portion of an integrated Electro-Magnetic Interference shield for the chip.

15. (Currently amended) A chip package comprising:

at least one chip; and

a package substrate for the chip comprising a first surface having a ball grid array of a plurality of solder balls adapted to come into contact with a printed wire board (PWB) and a second surface having at least one contact pad adapted to be electrically connected to the PWB, wherein the at least one chip is mounted onto the second surface of the package substrate.

16. (Original) The chip package as defined in claim 15, wherein the first surface is substantially orthogonal to the second surface.

17. (Original) The chip package as defined in claim 15, wherein the first surface is substantially parallel to the second surface.

18. (Previously presented) The chip package as defined in claim 15, wherein the at least one contact pad is configured to be located distally to the PWB and the ball grid array is configured to be located proximally to the PWB when the package substrate is in contact with the PWB.

19. (Currently amended) A method for interconnecting a chip package to a printed wiring board (PWB), the chip package comprising at least one chip and a package substrate for the chip including a first surface having a ball grid array (BGA) of a plurality of solder balls and a second surface having at least one contact pad, wherein the at least one chip is mounted onto the package substrate, the method comprising:

connecting the first surface of the package substrate of the chip package to the PWB via the plurality of solder balls of the BGA; and

connecting the second surface of the package substrate of the chip package to the PWB via at least one bridge lead.

20. (Currently amended) An apparatus for interconnecting a chip package to a printed wiring board (PWB), the chip package comprising at least one chip and a package substrate for the chip including a first surface having a ball grid array (BGA) of a plurality of solder balls and a second surface having at least one contact pad, wherein the at least one chip is mounted onto the package substrate, the apparatus comprising:

means for connecting the first surface of the package substrate of the chip package to the PWB via the plurality of solder balls of the BGA; and

means for connecting the second surface of the package substrate of the chip package to the PWB.

21. (Original) The apparatus as defined in claim 20, wherein the means for connecting the second surface comprises at least one bridge lead.

22. (Original) The apparatus as defined in claim 21, wherein the at least one bridge lead comprises at least one flying lead style of bridge lead.

23. (Original) The apparatus as defined in claim 21, wherein the at least one bridge lead comprises at least one edge wiping style of bridge lead.

24. (Original) The apparatus as defined in claim 21, wherein the at least one bridge lead comprises at least one top wiping style of bridge lead.

25. (Original) The apparatus as defined in claim 21, wherein the at least one bridge lead comprises at least one double wiping style of bridge lead.

26. (Original) The apparatus as defined in claim 25, wherein the at least one bridge lead further comprises a heat sink and thermal interface material for extracting heat from the chip.

27. (Original) The apparatus as defined in claim 25, wherein the at least one bridge lead further comprises at least a portion of an integrated Electro-Magnetic Interference shield for the chip.

28. (Currently amended) An apparatus for interconnecting a chip package to a printed wiring board (PWB), the chip package comprising at least one chip and a package substrate for the chip including a first surface having a ball grid array (BGA) of a plurality of solder balls adapted to be located between the chip package and the PWB and a second surface having at least one contact pad, wherein the at least one chip is mounted onto the package substrate, the apparatus comprising:

at least one bridge lead for connecting the at least one contact pad on the second surface of the package substrate of the chip package to the PWB.

29. (Original) The apparatus as defined in claim 28, wherein the at least one bridge lead comprises at least one flying lead style of bridge lead.

30. (Original) The apparatus as defined in claim 28, wherein the at least one bridge lead comprises at least one edge wiping style of bridge lead.

31. (Original) The apparatus as defined in claim 28, wherein the at least one bridge lead comprises at least one top wiping style of bridge lead.

32. (Original) The apparatus as defined in claim 28, wherein the at least one bridge lead comprises at least one double wiping style of bridge lead.

33. (Original) The apparatus as defined in claim 32, wherein the at least one bridge lead further comprises a heat sink and thermal interface material for extracting heat from the chip.

34. (Original) The apparatus as defined in claim 32, wherein the at least one bridge lead further comprises at least a portion of an integrated Electro-Magnetic Interference shield for the chip.

35. (Currently amended) An electronic interconnection system comprising:

a printed wiring board (PWB) having an interconnection area;

a package substrate for a chip, the package substrate having a first surface and a second surface, the first surface configured to be in contact with the interconnection area to allow communication signals between the ~~package substrate~~ chip and the PWB, the second surface having a contact pad electrically connected to the chip; and

a bridge lead for electrically connecting the contact pad of the package substrate with the PWB.

36. (Currently amended) An electronic interconnection system comprising:

a printed wiring board (PWB) having an interconnection area;

a package substrate for a chip, the package substrate having a first surface and a second surface, the first surface configured to be in contact with the interconnection area to allow

communication signals between the package substrate and the PWB, the second surface having a contact pad; and

a bridge lead for electrically connecting the contact pad of the package substrate with the PWB, wherein the bridge lead increases an amount of electrical signals between the ~~package substrate~~ chip and the PWB.